REMARKS

Claim rejection 35 USC § 112

Concerning items 2 and 3, relating to an alleged lack of support in the specification, there is a passage at page 12 which states "Within each pointer byte the pointer value is transmitted in a 5 bit field and indicates the number of the first time slot of the E1/T1 transmitted in the node 125 µs frame." Nevertheless claim 14 has been amended to remove the text indicating "the number ". Claim 15 does not contain this limitation. If this rejection is maintained, more explanation of which part of the claim is not supported would be appreciated.

Concerning items 4, 5 and 6, claim amendments have been made to address these points.

Claim rejections 35 USC § 103

Concerning items 7 onwards about obviousness, the following comments are made. The two independent claims 2 and 9 stand rejected under 35 USC § 103(a) over Won and Irwin and Caves. These claims and therefore all the claims have the features of:

      a) "pointers identifying phase of the TDM traffic"

      b) "said pointers are mapped into one or more separate asynchronous cells for transport ahead of said traffic cells."

The question of whether these features are disclosed could determine the outcome for all claims and so is considered first. The Examiner asserts that feature b) is shown by Irwin and helpfully provides more explanation in support of the assertion. Now that this assertion is better understood, it is respectfully traversed for the following reasons. Irwin in Figure 5 shows a switch which receives ATM cells at an input side 415 shown on the left of the figure, and outputs switched cells at the right of the figure. In the ATM headers of the ATM cells there are identifiers to enable a

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TDM frame spread across the payload of several ATM cells to be recovered correctly even if the cells are not received in the same order that they are sent. Such reordering takes place in async cell buffer 460. It is acknowledged at lines 47-50 of col 14 that:

"The queueing characteristics of the ATM switch removes any fixed timing relationship between a cell arrival and the synchronous 8 kHz rate used to interconnect isochronous services."

The timing of the TDM data is restored by another block in fig 5, as explained at lines 50 to 53 of col 14:

"To restore the relationship of channels to the 8 kHz frame structure, a block of memory, exemplified as the DS0 TSIC 420 may be used to reassemble the TDM frame structure."

The DS0 420 outputs ATM payloads to line 413 in fig 5 where ATM headers are added to create ATM cells for output. In Irwin, the headers of incoming cells are separated before the reordering of the payloads. Even if the "identifiers" of Irwin were to be considered as equivalent to an example of the claimed pointers (which need not be admitted or addressed now), there is no disclosure of the claim feature of mapping them to separate cells for transport ahead of the traffic. Instead, in Irwin, the headers containing the identifiers are separated and placed on a header bus 414. Lines 46 onwards of col 13 explain that:

"The input controller 480 receives header information for each incoming cell from the header bus 414 and provides operating instructions for the asynchronous cell buffer 460...."

The input controller also provides information to the output controller 490 which is for "providing an outgoing header for each cell delivered from the buses 444 and 413..." (lines 46 onwards of col 13). As there is no suggestion that the "identifiers" are sent in separate cells ahead of their corresponding payload, it can only be inferred that if "identifiers" are output at all, these "identifiers" must be placed in the outgoing header attached to their payload. Otherwise the outgoing ATM cells could not be reordered by a corresponding process at the next ATM switch.

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Hence it cannot be inferred from Irwin that the "identifiers" could be sent ahead in separate cells. The identifiers are only separated from their payload within the switch, and are passed to the input controller as a header data stream which consists of octets 01-05, (lines 2 and 3 of col 13). This header datastream is described as high speed and having cells, but such cells are not asynchronous cells. Furthermore, this header datastream is not cells "for transport" as claimed, since it is purely internal to the switch. Hence there is no disclosure of claim feature b) by Irwin.

It would not have been obvious to alter Irwin or any of the prior art to send the identifiers in separate asynchronous cells ahead of the payload because in Irwin there needs to be an identifier for each cell (unlike the pointers claimed) and it would involve additional effort and complication in the switch to determine which identifier belongs to which cell. In contrast, where, as claimed, the pointers indicate phase information rather than merely cell order as in Irwin, there are advantages in sending such TDM phase information ahead in separate asynchronous cells. The TDM phase information can apply to more than one cell and so need not be sent with every cell, and so there is an advantage in sending it separately. For example the phase information can be sent as values with more bits and so have more precision without overflowing the header for example. Furthermore, bandwidth need not be wasted since it "facilitates the avoidance of the need for sending the pointer cells every 125μs frame if these are not required..." (page 14) and can avoid sending the same information repeatedly for many cells. There is no suggestion of feature b) nor the advantages it can bring, in any of the cited prior art, taken singly or in combination. Hence all the claims involve nonobvious features.
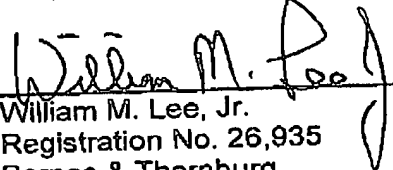
In conclusion, the disclosure of Irwin of including cell ordering information in cell headers is not relevant to the claim features missing from Won relating to sending TDM phase information. Since Irwin fails to teach the features missing from Won, even if one of ordinary skill in the art were to combine Won with Irwin, he would not

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arrive at a method having all of the limitations set forth in claim 2. Thus, claim 2 must be non-obvious. For the same reasons, the subject matter of apparatus claim 9 is non-obvious. All dependent claims are considered to be patentable at least by virtue of their dependency on claims 2 or 9.

All the points raised by the Examiner have now been met and favorable reconsideration is requested. For the foregoing reasons, applicants respectfully submit that the claims in this application are in condition for allowance. Early issuance of a Notice of Allowance is solicited.

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